

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1973731	(wafer substrate chip IC (integrated near5 circuit))	US-PGPU B; USPAT; USOCR	OR	ON	2006/01/19 12:22
L2	488874	1 and (vacuum suc\$3)	US-PGPU B; USPAT; USOCR	OR	ON	2006/01/19 12:23
L3	605600	1 and (vacuum suc\$4)	US-PGPU B; USPAT; USOCR	OR	ON	2006/01/19 12:23
L4	4046	3 and (PSA (pressure near5 senistive near5 tape))	US-PGPU B; USPAT; USOCR	OR	ON	2006/01/19 12:24
L5	1052	4 and porous	US-PGPU B; USPAT; USOCR	OR	ON	2006/01/19 12:19
L6	712	5 and (dic\$3 cut\$4 saw\$3 singulat\$3)	US-PGPU B; USPAT; USOCR	OR	ON	2006/01/19 12:20
L7	122	6 and semiconductor	US-PGPU B; USPAT; USOCR	OR	ON	2006/01/19 12:20
L8	2013684	(wafer substrate chip IC (integrated near5 circuit))	EPO; JPO; DERWENT ; IBM_TDB	OR	ON	2006/01/19 12:22
L10	86462	8 and (vacuum suc\$4)	EPO; JPO; DERWENT ; IBM_TDB	OR	ON	2006/01/19 12:23
L11	9	10 and (PSA (pressure near5 senistive near5 tape))	EPO; JPO; DERWENT ; IBM_TDB	OR	ON	2006/01/19 12:24

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	0	((groove recess mesa open\$3 trench) same (wafer substrate IC chip) same (PSA (pressure near5 sensitiv5) near5 (adhesive tape)) same (cut\$3 dic\$3 singulat\$3) same porous same (peel\$3 remov\$3) same (suc\$4 vacuum\$3)).clm.	US-PGPU B	OR	ON	2006/01/19 14:08
L2	0	((groove recess mesa open\$3 trench) same (wafer substrate IC chip) same (PSA (pressure near5 sensitiv5) same (adhesive tape)) same (cut\$3 dic\$3 singulat\$3) same porous same (peel\$3 remov\$3) same (suc\$4 vacuum\$3)).clm.	US-PGPU B	OR	ON	2006/01/19 14:10
L3	1	((groove recess mesa open\$3 trench) and (wafer substrate IC chip) and (PSA (pressure near5 sensitiv5) and (adhesive tape)) and (cut\$3 dic\$3 singulat\$3) and porous and (peel\$3 remov\$3) and (suc\$4 vacuum\$3)).clm.	US-PGPU B	OR	ON	2006/01/19 14:11